What is claimed is:

1. An add-compare-select apparatus for a Viterbi decoder with a constraint length of K, comprising:

a subtractor for calculating a path metric difference by subtracting a path metric of state S_q at instant $i-1$ from another path metric of state S_p at instant $i-1$, where said path metrics are represented by α bits of precision;

a λ-bit multiplexer for selectively providing an output between λ least significant bits of a branch metric difference at instant i and the negative thereof according to a select signal, where said branch metric difference is represented by β bits of precision and $\beta=\lambda+1$;

a λ-bit unsigned comparator for yielding a comparison result by comparing the magnitude of λ least significant bits of said α-bit path metric difference and the magnitude of said λ-bit multiplexer output;

a first combinational-logic circuit for logically operating δ most significant bits of said α-bit path metric difference and a sign bit of said branch metric difference at instant i to predetermine whether the magnitude of said α-bit path metric difference is greater than that of said branch metric difference, setting a decision bit of state S_u at instant i based on a predetermination made therein if said predetermination is met, and setting said

decision bit of state S_u at instant i to be consistent with said comparison result if said predetermination is not met, where $\delta = \alpha - \lambda$;

a second combinational-logic circuit for logically operating δ most significant bits of said α-bit path metric difference and said sign bit of said branch metric difference at instant i to predetermine whether the magnitude of said α-bit path metric difference is greater than that of the negative of said branch metric difference, setting a decision bit of state S_v at instant i based on another predetermination made therein if said another predetermination is met, and setting said decision bit of state S_v at instant i to be consistent with said comparison result if said another predetermination is not met;

a first adding means, according to said decision bit of state S_u at instant i, for calculating a new path metric for state S_u at instant i by selectively adding said path metric of state S_q at instant $i-1$ and a branch metric of a transition from state S_q to state S_u at instant i or adding said another path metric of state S_p at instant $i-1$ and another branch metric of a second transition from state S_p to state S_u at instant i, where said branch metrics are represented by λ bits of precision; and

a second adding means, according to said decision bit of state S_v at instant i, for calculating another new path metric for state S_v at instant i by

selectively adding said path metric of state S_q at instant $i-1$ and said another branch metric of said second transition from state S_p to state S_u at instant i or adding said another path metric of state S_p at instant $i-1$ and said branch metric of said transition from state S_q to state S_u at instant i;

wherein said branch metric difference is pre-calculated by subtracting said another branch metric of said second transition from state S_p to state S_u at instant i from said branch metric of said transition from state S_q to state S_u at instant i;

wherein states S_p and S_q at instant $i-1$ and states S_u and S_v at instant i are organized in a butterfly trellis structure, and subscripts p, q, u and v are given by:

$$p = 0,\ 1,\ 2,\ldots,\ 2^{K-2}-1$$
$$q = 2^{K-2}+p$$
$$u = 2p$$
$$v = 2p+1.$$

2. The apparatus as recited in claim 1 wherein said first combinational-logic circuit is capable of setting said select signal depending on whether said branch metric difference at instant i and said path metric difference at instant $i-1$ both have the same sign.

3. The apparatus as recited in claim 1 wherein said second combinational-logic circuit is capable of setting said select signal depending on whether said branch metric

difference at instant i and said path metric difference at instant $i-1$ both have the same sign.

4. The apparatus as recited in claim 1 further comprising means for predetermining a local winner state between states S_u and S_v at instant i based on said decision bits of states S_u and S_v at instant i, and the sign of said path metric difference at instant $i-1$ or the sign of said branch metric difference at instant i, whereby a saving of half the output number of said new path metrics at instant i is achieved.

5. An apparatus for branch metric computation and add-compare-select operation in a rate $1/n$ Viterbi decoder with a constraint length of K, comprising:

a branch metric generator receiving a data symbol including n decision metrics in Q-bit representation, for calculating a plurality of branch metrics each of which is a measure between said currently received data symbol and a corresponding branch label, and further pre-calculating a branch metric difference by subtracting a first branch metric of a transition from state S_p to state S_u at instant i from a second branch metric of another transition from state S_q to state S_u at instant i; and

an add-compare-select unit receiving said first branch metric of said transition from state S_p to state S_u, said second branch metric of said another transition from state S_q to state S_u and said branch metric difference at instant i from said

branch metric generator and calculating a path metric difference between a path metric of state S_p at instant $i-1$ and another path metric of state S_q at instant $i-1$, for respectively setting decision bits of states S_u and S_v at instant i based on said branch metric difference at instant i and said path metric difference, comprising:

a first adding means, according to said decision bit of state S_u at instant i, for calculating a new path metric for state S_u at instant i by selectively adding said another path metric of state S_q at instant $i-1$ and said second branch metric of said another transition from state S_q to state S_u at instant i or adding said path metric of state S_p at instant $i-1$ and said first branch metric of said transition from state S_p to state S_u at instant i;

a second adding means, according to said decision bit of state S_v at instant i, for calculating another new path metric for state S_v at instant i by selectively adding said another path metric of state S_q at instant $i-1$ and said first branch metric of said transition from state S_p to state S_u at instant i or adding said path metric of state S_p at instant $i-1$ and said second branch metric of said another transition from state S_q to state S_u at instant i; and

means for selectively outputting one of said new path metrics, which is a survivor path metric of a local winner state, by predetermining said local winner state between states S_u and S_v at instant i based on said decision bits of states S_u and S_v at instant i, and the sign of said path metric difference at instant $i-1$ or the sign of said branch metric difference at instant i;

wherein states S_p and S_q at instant $i-1$ and states S_u and S_v at instant i are organized in a butterfly trellis structure, and subscripts p, q, u and v are given by:

$$p = 0,\ 1,\ 2,\ldots,\ 2^{K-2}-1$$
$$q = 2^{K-2} + p$$
$$u = 2p$$
$$v = 2p+1.$$

6. The apparatus as recited in claim 5 wherein said add-compare-select unit further comprises:

a subtractor for calculating said path metric difference by subtracting said another path metric of state S_q at instant $i-1$ from said path metric of state S_p at instant $i-1$, where said path metrics are represented by α bits of precision, respectively;

a λ-bit multiplexer for selectively providing an output between λ least significant bits of said branch metric difference at instant i and the negative thereof according to a select signal, where said

branch metric difference is represented by β bits of precision and $\beta = \lambda + 1$;

a λ-bit unsigned comparator for yielding a comparison result by comparing the magnitude of λ least significant bits of said α-bit path metric difference and the magnitude of said λ-bit multiplexer output;

a first combinational-logic circuit for logically operating δ most significant bits of said α-bit path metric difference and a sign bit of said branch metric difference at instant i to predetermine whether the magnitude of said α-bit path metric difference is greater than that of said branch metric difference, setting said decision bit of state S_u at instant i based on a predetermination made therein if said predetermination is met, and setting said decision bit of state S_u at instant i to be consistent with said comparison result if said predetermination is not met, where $\delta = \alpha - \lambda$; and

a second combinational-logic circuit for logically operating δ most significant bits of said α-bit path metric difference and said sign bit of said branch metric difference at instant i to predetermine whether the magnitude of said α-bit path metric difference is greater than that of the negative of said branch metric difference, setting said decision bit of state S_v at instant i based on another predetermination made therein if said another predetermination is met, and setting

said decision bit of state S_v at instant i to be consistent with said comparison result if said another predetermination is not met.

7. The apparatus as recited in claim 6 wherein said first combinational-logic circuit is capable of setting said select signal depending on whether said branch metric difference at instant i and said path metric difference at instant $i-1$ both have the same sign.

8. The apparatus as recited in claim 6 wherein said second combinational-logic circuit is capable of setting said select signal depending on whether said branch metric difference at instant i and said path metric difference at instant $i-1$ both have the same sign.

9. The apparatus as recited in claim 6 wherein said branch metrics are represented by λ bits of precision, in which λ is given by:

$$\lambda = Q + n - 1$$

10. The apparatus as recited in claim 9 wherein the number of bits of precision representing said path metrics, α, is given by:

$$\alpha = 1 + \left\lceil \log_2 \left(n \cdot K \left(2^Q - 1 \right) \right) \right\rceil$$

where $\lceil \cdot \rceil$ denotes a ceiling function.

11. The apparatus as recited in claim 5 further comprising:

a dummy insertion unit for performing a dummy insertion procedure inverse to a bit-stealing procedure in

a transmitter according to a puncturing pattern and outputting a dummy insertion flag to indicate a position at which a dummy value is inserted into said decision metrics.

12. The apparatus as recited in claim 11 wherein said branch metric generator ignores said inserted dummy value in response to said dummy insertion flag when calculating said branch metrics for said n decision metrics including said inserted dummy value.

13. A rate $1/n$ Viterbi decoder with a constraint length of K, comprising:

a dummy insertion unit for performing a dummy insertion procedure, which is inverse to a bit-stealing procedure in a transmitter, on a sequence of decision metrics in Q-bit representation according to a puncturing pattern and outputting a dummy insertion flag to indicate a position at which a dummy value is inserted into said decision metrics;

a branch metric generator receiving n number of said decision metrics including said dummy value to group into a data symbol, for calculating a plurality of branch metrics each of which is a measure between said data symbol and a corresponding branch label, and further pre-calculating a branch metric difference for a pth sub-group of states including states S_p, S_q, S_u and S_v by subtracting a first branch metric of a transition from state S_p to state S_u at instant i

from a second branch metric of another transition from state S_q to state S_u at instant i, wherein said dummy value is ignored in response to said dummy insertion flag when said branch metrics are calculated for said data symbol;

P add-compare-select units, in which a pth add-compare-select unit receives said first branch metric of said transition from state S_p to state S_u, said second branch metric of said another transition from state S_q to state S_u and said branch metric difference for the pth sub-group of states at instant i from said branch metric generator and calculates a path metric difference between a path metric of state S_p at instant $i-1$ and another path metric of state S_q at instant $i-1$, for setting a pair of decision bits for states S_u and S_v at instant i based on said branch metric difference at instant i and said path metric difference, respectively generating new path metrics for states S_u and S_v at instant i, further predetermining a local winner state between states S_u and S_v at instant i based on said decision bits of states S_u and S_v at instant i, and the sign of said branch metric difference at instant i or the sign of said path metric difference, and providing one of said new path metrics as output, which is a survivor path metric of said local winner state at instant i, to achieve a saving of half the output number of said new path metrics; and

a survivor memory unit receiving said P survivor path metrics of said P local winner states and said P pairs of decision bits at instant i from said P add-compare-select units, for storing survivor path sequences and yielding a decoded bit sequence;

wherein states S_p and S_q at instant $i-1$ and states S_u and S_v at instant i are organized in a butterfly trellis structure, and subscripts p, q, u and v are given by:

$$p = 0,\ 1,\ 2,\ \ldots,\ P-1$$

$$q = P + p$$

$$u = 2p$$

$$v = 2p + 1$$

where $P = 2^{K-2}$.

14. The Viterbi decoder as recited in claim 13 wherein the pth add-compare-select unit comprises:

a subtractor for calculating said path metric difference by subtracting said another path metric of state S_q at instant $i-1$ from said path metric of state S_p at instant $i-1$, where said path metrics are represented by α bits of precision, respectively;

a λ-bit multiplexer for selectively providing an output between λ least significant bits of said branch metric difference at instant i and the negative thereof according to a select signal, where said branch metric difference is represented by β bits of precision and $\beta = \lambda + 1$;

a λ-bit unsigned comparator for yielding a comparison result by comparing the magnitude of λ least significant bits of said α-bit path metric difference and the magnitude of said λ-bit multiplexer output;

a first combinational-logic circuit for logically operating δ most significant bits of said α-bit path metric difference and a sign bit of said branch metric difference at instant i to predetermine whether the magnitude of said α-bit path metric difference is greater than that of said branch metric difference, setting said decision bit of state S_u at instant i based on a predetermination made therein if said predetermination is met, and setting said decision bit of state S_u at instant i to be consistent with said comparison result if said predetermination is not met, where $\delta = \alpha - \lambda$; and

a second combinational-logic circuit for logically operating δ most significant bits of said α-bit path metric difference and said sign bit of said branch metric difference at instant i to predetermine whether the magnitude of said α-bit path metric difference is greater than that of the negative of said branch metric difference, setting said decision bit of state S_v at instant i based on another predetermination made therein if said another predetermination is met, and setting said decision bit of state S_v at instant i to be

consistent with said comparison result if said another predetermination is not met.

15. The Viterbi decoder as recited in claim 14 wherein the pth add-compare-select unit further comprises:

a first adding means, according to said decision bit of state S_u at instant i, for calculating said new path metric of state S_u at instant i by selectively adding said another path metric of state S_q at instant $i-1$ and said second branch metric of said another transition from state S_q to state S_u at instant i or adding said path metric of state S_p at instant $i-1$ and said first branch metric of said transition from state S_p to state S_u at instant i; and

a second adding means, according to said decision bit of state S_v at instant i, for calculating said new path metric of state S_v at instant i by selectively adding said another path metric of state S_q at instant $i-1$ and said first branch metric of said transition from state S_p to state S_u at instant i or adding said path metric of state S_p at instant $i-1$ and said second branch metric of said another transition from state S_q to state S_u at instant i.

16. The Viterbi decoder as recited in claim 14 wherein said first combinational-logic circuit is capable of setting said select signal depending on whether said branch metric difference at instant i and said path metric difference at instant $i-1$ both have the same sign.

17. The Viterbi decoder as recited in claim 14 wherein said second combinational-logic circuit is capable of setting said select signal depending on whether said branch metric difference at instant i and said path metric difference at instant $i-1$ both have the same sign.

18. The Viterbi decoder as recited in claim 14 wherein said branch metrics are represented by λ bits of precision, in which λ is given by:

$$\lambda = Q + n - 1$$

19. The Viterbi decoder as recited in claim 14 wherein the number of bits of precision representing said path metrics, α, is given by:

$$\alpha = 1 + \left\lceil \log_2 \left(n \cdot K \left(2^Q - 1 \right) \right) \right\rceil$$

where $\lceil \cdot \rceil$ denotes a ceiling function.

20. The Viterbi decoder as recited in claim 13 wherein said decision metrics are hard-decision data if quantized to one bit of precision.